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PATENT APPLICATION

ATTORNEY DOCKET NO. 10015698-4

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Blaine D. Gaither

Serial No.: 10/649,917 Examiner: Bradley, Matthew A.

Filing Date: 08/26/2003 Group Art Unit: 2187

Title: CACHE SYSTEM WITH GROUPS OF LINES AND WITH COHERENCY FOR BOTH SINGLE LINES AND GROUPS OF LINES

REMARKS IN RESPONSE TO OFFICE ACTION

COMMISSIONER FOR PATENTS
P.O. Box 1450
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Sir:

No amendments have been made. Claims 1, 3-4 and 7-10 remain in the application. Claims 4 and 8-10 have been allowed or declared allowable. Reexamination and reconsideration is respectfully requested.

In the paper mailed 10/18/2006, claims 1, 3, and 7 were rejected under 35 USC 102(e) as being anticipated by US Patent Number 6,374,332 (Mackenthun *et al.*). Applicant respectfully traverses.

Claim 1 specifies a cache memory that reads and caches a group of lines with a single memory transaction and claim 7 specifies retrieving a group of lines in response to a request for a single line. The examiner cites Mackenthun *et al.* column 12, lines 26-30, for a cache memory that reads and caches a group of lines with a single memory transaction and for retrieving a group of lines in response to a request for a single line. The cited lines have nothing to do with reading and caching a group of lines, much less reading and caching a group of lines with a single memory transaction. From the abstract, Mackenthun *et al.* allow multiple simultaneous requests for ownership. Requests for ownership is not